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AMENDMENTS TO THE CLAIMS:

Claim 1:

1. (Currently Amended) A clock and data recovery unit for recovering a received serial data bit stream having:

(a) phase adjustment means for adjustment of a sampling time in the center of a unit interval of the received data bit stream, wherein the phase adjustment means comprises:

(a1) means for generating equidistant reference phase signals;

(a2) a phase interpolation unit which rotates the generated reference phase signals with a predetermined granularity in response to a rotation control signal;

(a3) an oversampling unit for oversampling the received data bit stream with the rotated reference phase signals according to a predetermined oversampling rate;

(a4) a serial-to-parallel-conversion unit which converts the oversampled data bit stream into a deserialized data bit stream with a predetermined decimation factor;

(a5) a binary phase detection unit for detecting an average phase difference between the received serial data bit stream and the rotated reference phase signal by adjusting a phase detector gain depending on an actual

data density of the deserialized data bit stream such that the variation of the average phase detection gain is minimized; and

(a6) a loop filter for filtering the detected average phase difference to generate the rotation control signal for the phase interpolation unit;

(b) data recognition means for recovery of the received data bit stream which includes a number of parallel data recognition FIR-Filters, wherein each data recognition FIR-Filter comprises:

(b1) a weighting unit for weighting data samples of the deserialized data bit stream around the sampling time adjusted by the phase adjustment means;

(b2) a summing unit for summing up the weighted data samples; and

(b3) a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

Claim 31:

31. (Currently Amended) Method for clock and data recovery of a received serial data bit stream comprising the following steps:

(a) adjusting a sampling time in the center of a unit interval of a received data bit comprising the following substeps:

(a1) generating reference phase signals;

(a2) rotating said [~~generated~~] reference phase signals in response to a rotation control signal;

~~(a2)~~ (a3) oversampling the received data bit stream with the rotated reference phase signals;

~~(a3)~~ (a4) converting an oversampled data bit stream into a deserialized data stream;

~~(a4)~~ (a5) detecting an average phase difference between the received serial data bit stream and the rotated phase signals by adjusting a phase detector gain depending on a data density of the deserialized data stream to minimize the variation of an average phase detector gain;

~~(a5)~~ (a6) filtering the detected phase difference to generate the rotation control signal; [[.]]

(b) recovering the received data bit stream comprising the following substeps:

(b1) weighting data samples of the deserialized data stream around the adjusted sampling time;

(b2) summing up the weighted data samples;

(b3) comparing the summed up weighted data samples with a threshold value to detect the logic value of a data bit within the serial data bit stream.